Analysis of the Source Inductance Effect on the Power Performance of High Development HEMT's in the *Ka*-Band

C. Gaquiere, *Student Member, IEEE,* B. Bonte, D. Théron, Y. Crosnier, and J. Favre

***Abstract*— This paper provides an analysis of the power performance degradations of interdigitated HEMT's in millimeter wave range as the total gate width increases. It investigates the possibility of optimizing the device topologie by combining a limited number of via holes and airbridge source connections in order to offer a good cost-performance trade-off.**

I. Introduction

FET's with a total gate width higher than 10 mm and an output power of a few watts [1] are commonly fabricated for lower frequencies essentially in the L band (wireless communication). At higher frequencies large gate widths result in gain, efficiency, and power density degradations essentially due to the attenuation along each gate finger [2], the phase variation between the different gate fingers and the increasing parasitic effect of the capacitances and source inductance.

These effects become more important in millimeter wave range. The state of the art is of 800 mW at 44.5 GHz for a device of 1.8-mm total gate width with little via holes under each source finger [3]. Such a performance involves a very impressive technological sophistication which cannot be easily developed in the frame of an industrial production.

From this viewpoint, we think that a technology making use of air bridge relays would be a good alternative provided that the parasitic effects related to that technique could be minimized. This question constitutes the central objective of the present study. This one is mainly focused on the analysis of a lot of devices realized on the same wafer with scaling variations in order to quantify the effect of the topology on the power performances.

II. Device Description

The device used in this work is a pseudomorphic 0.25 μm T shape gate heterostructure FET. The layer was grown by molecular beam epitaxy. It consists of a AlGaAs/InGaAs/GaAs heterojunction structure with a single silicon doping plane in the AlGaAs. In this work, four gate topologies were studied: 2 × 50, 4 × 50, 6 × 50, 8 × 50 μm. The source fingers are interconnected with air bridges and their grounding is realized with two via holes placed at each extremity of the device. These via holes are etched through the 100-μm-thick substrate. The main DC characteristics of the devices were a drain current density of 650 mA/mm at $V_{gs} = 0.5$ V, a breakdown voltage of 7.5 V in diode configuration and 4.8 V in transistor configuration at open channel. These voltages were obtained at 1 mA/mm of gate current.

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C. Gaquiere, B. Bonte, D. Théron, and Y. Crosnier are with the Institut d'Electronique et de Microélectronique du Nord, U.M.R.-C.N.R.S. 9929, Département Hyperfréquences et Semiconducteurs, 59652 Villeneuve d'Ascq Cedex, France.

J. Favre is with the THOMSON-CSF Semiconducteurs Spécifiques, 91401 Orsay Cedex.

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III. Device Performance

The microwave characteristics of the device were determined from S parameter measurements performed with a HP85107 Network Analyser and a Cascade Microtech probe system at frequencies from 1–36 GHz. The Network Analyser was calibrated using a TRM standard and the equivalent circuit was extracted using the classical Dambrine method [4]. All the studied devices presented the same pinch off voltage (Fig. 1). This made possible the comparison of their small signal equivalent circuits. Values of the main intrinsic and extrinsic elements of their equivalent lumped circuits are summarized in Table I. The variations of these elements follow normal scaling rules versus the different gate widths except for the source inductance element which increases linearly with the total gate width. This behavior suggests that the source inductance origin has to be mainly attributed to the air bridge ribbon. Calculations were performed with these elements on the basis of the usual relationship of the maximum available gain cutoff frequency [5], shown in the equation at the bottom of the next page.

A drastic decrease of this quantity versus the total gate width was found (Fig. 2). Given that in the F_{mag} relationship the source inductance L_s is the only element which varies in a way opposite to the normal scaling rules, the decrease of F_{mag} is likely to be due to this element.

IV. Discussion

In order to confirm that the effect of the source inductance is the main reason for the power gain degradation, we will now examine the impact of this source inductance on the FET input impedance.

A basic equivalent unilateral circuit of the FET was used. We checked the validity of this model by calculating the ratio $G_m{*}C_{gd}/G_d{*}C_{gs}$ which is constant versus the total gate width (Table II). This term is the only one that contains the feedback

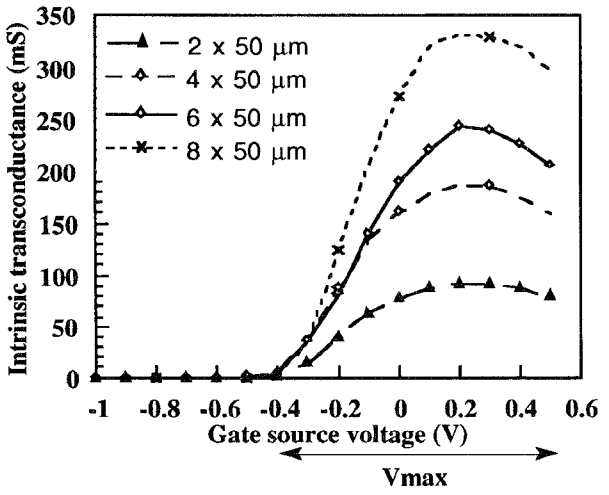

Fig. 1. Transconductance versus gate bias voltage for different gate widths.

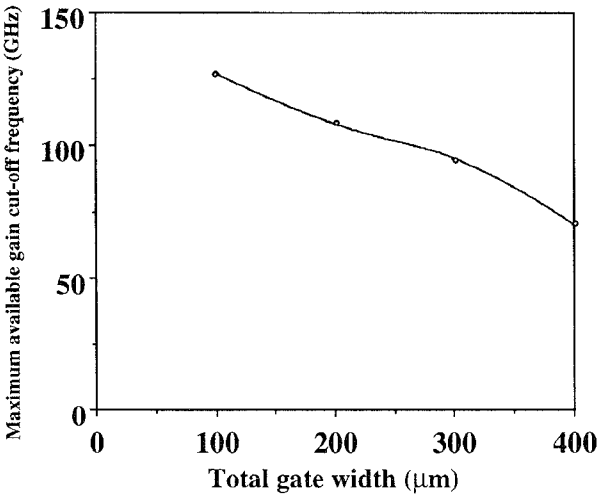

Fig. 2. Maximum calculated available gain cutoff frequency behavior versus the total gate width.

TABLE I
EVOLUTION OF MAINS ELEMENTS OF THE ELECTRICAL EQUIVALENT CIRCUIT (INTRINSIC AND EXTRINSIC)

	Gm(mS)	C_{gs} (fF)	Gd (mS)	Cgd (fF)	Ri(Ω)	Fc(GHz)
2x50µm	84	112	4 5	18	6 5	119
4x50µm	170	230	9.5	40	2 5	118
6x50µm	242	339	15.3	60	1.9	114
8x50µm	339	462	20 6	84	1 5	116

	Rs (Ω)	Rd (Ω)	Rg (Ω)	Ls (pH)	Ld (pH)	Lg (pH)	Cpg (fF)	Cpd (fF)
2x50µm	4.1	3 8	3 2	2	100	80	40	40
4x50µm	2	2	1 9	8	90	85	40	40
6x50µm	1.2	1.2	1.2	12	85	80	40	40
8x50µm	0.9	0.9	0 9	16	85	80	40	40

capacitance C_{gd} in the F_{mag} expression, so it is justified to neglected this capacitance because it does not modified the Fmag degradation. Even though the L_s value remains relatively small, its effect on the power gain is dramatic since it induces at the gate termination an equivalent resistance [6]. Indeed using our basic unilateral FET configuration (Fig. 3), the maximum input power delivered to the gate of the DUT at saturation is approximatively

$$P_{\mathrm{in}} \cong \frac{|V_{gs}|^2 * R_{\mathrm{in}} * C_{gs}^2 * \omega^2}{4}$$

where $|V_{gs}|$ is the maximum magnitude peak to peak excursion of the gate source voltage: about 1 V in the present case (Fig. 1). The power gain degradation results directly from the increase of P_{in} due to the increase of R_{in}. As indicated R_{in} comprises a pure resistive term $R = R_g + R_i + R_s$ and the feedback term due to the source inductance L_s.

Table II shows the respective variations of these two terms versus the total gate width. R follows the scaling rule but it is by far not true for the $G_m * L_s/C_{gs}$ factor. Moreover this term becomes more and more important compared to R as the total gate width increases. The final result is that after a slight decrease, the total input resistance undergoes a rise. It is the fundamental reason of the power gain degradation.

TABLE II
INPUT RESISTANCE BEHAVIOR VERSUS THE TOTAL GATE WIDTH

	$\frac{Gm * Cgd}{Gd * Cgs}$	$\frac{Gm * Ls}{Cgs}$ (Ω)	R=Rg+Ri+Rs (Ω)	Re=R + $\frac{Gm * Ls}{Cgs}$ (Ω)
2x50µm	3	1.5	13 8	15 3
4x50µm	3 1	6	6.4	12.4
6x50µm	2.8	8 5	4.3	12 8
8x50µm	3	11 8	3 3	15.1

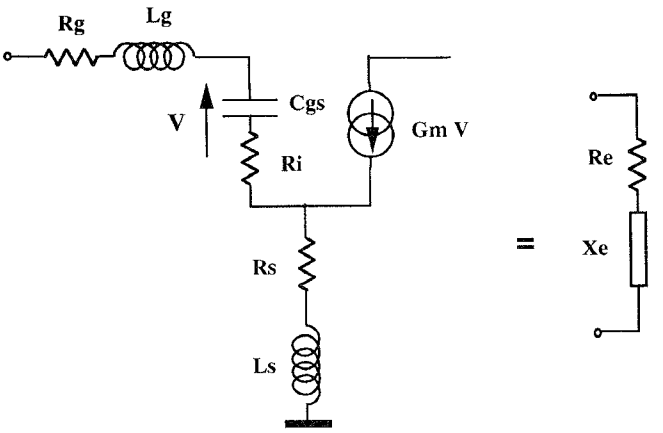

Fig. 3. Lumped equivalent circuit in first approximation of a FET

V. CONCLUSION

The influence of the source air bridge inductance in interdigitated millimeter wave HEMT's was analysed. The conclusion of this study is that high power FET's require a trade-off

$$F_{\mathrm{mag}} = \frac{F_C}{2 * \sqrt{G_d} * \sqrt{[R_s + R_g + (\pi * F_c * L_s)] + \left[\left(\frac{G_m * C_{gd}}{2 * G_d * C_{gs}}\right) * (R_s + R_g + (2 * \pi * F_c * L_s))\right]}}$$

between the number of via holes and the length and number of the air bridge source interconnections. In addition, it is clear that an accurate optimization of the width, height and position of the air bridges on the structure must be achieved to order to push away the limit of the power degradation.

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